von Neumann was not always right: design of reliable system is better to do with reliable components

Device & results chronology

RELIABLE DESIGN FROM RELIABLE COMPONENT

FAULT TOLERANT AVIONICS
Active safety system for aircraft with double Motorola 68020, fault tolerant memory for applications (41 chip of SRAM) and new triped memory together with flight data recorder with unique thermo-resistant system - were developed and tested.  
Completed 1994

ERRIC
Embedded recoverable reduced instruction computer was designed and prototyped in 1998-2008 before and within FP6 ONBASS project (www.onbass.org). Malfunction tolerance and rigorous design enabled to achieve fault tolerance with 12% structural redundancy and zero time redundancy. ERRIC requires 6.5 times less power than ARM and has similar performance.
1998-up to now

NEXT STOP - NEW ERA
Idea to combine ERRIC and our memory designs to make fault tolerant reconfigurable architecture on a wafer became known as ERA (evolving reconfigurable architecture).
In progress

Triplicated memory (TRAM) - right picture was developed in 1992.
Malfunction tolerance of the device is unique.